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PART NO. : **MS-10-2004F**

FOR MESSRS. :

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3. Precautions for LCM

3-1 Precautions in handling LCD Modules (hereinafter LCM's)

EVERBOUQUET INTERNATIOAL CO., LTD. technology's LCM's have been assembled and accurately calibrated before delivery.

Please observe the following criteria when handling.

A. Do not subject the module to excessive shock.

B. Do not modify the tab on the metal holder.

C. Do not tamper with the printed circuit board.

D. Limit soldering of the printed circuit board to I/O terminals only.

E. Do not touch the zebra strip nor modify its location.

3-2 Static electricity warning:

EVERBOUQUET INTERNATIONAL CO., LTD. LCM uses CMOS LSI technology. Therefore, strict measures to avoid static electricity discharge are followed through all processes from manufacturing through shipping. When handling an LCM, take sufficient care to prevent static electricity discharge as you would any CMOS IC.

A. Do not take the LCM from its anti-static bag until it's to be assembled. LCM's are individually packaged in bags specially treated to resist static electricity. When storing, keep the LCM packed in the original bags, or store them in a container processed to be resistant to static electricity, or in an electric conductive container.

B. Always use a ground strap when handling a LCM.
Always use a ground strap while working with the module, from the time it is taken out of the anti-static bag until it is assembled. When it is necessary to transfer the LCM, once it has been taken out of the bag, always place it in an electric conductive container. Avoid wearing clothes made of chemical fibers, the use of cotton or conductive treated fiber clothing is recommended.

C. Use a no-leak iron for soldering the LCM.
The soldering iron to be used for soldering the I/O terminals to the LCM are to be insulated or grounded at the iron tip.

D. Always ground electrical apparatuses required for assembly.
Electrical apparatuses required to assemble the LCM into a product, i.e. electrical screw drivers are to be first grounded to avoid transmitting spike noises from the motor.

E. Assure that the work bench is properly grounded.

F. Peel off the LCM protective film slowly. The module is attached with a film to protect the display surface from contamination, damage, adhesion of flux, etc. Peeling off this film abruptly could case static electricity to be generated, so peel the tape slowly.

G. Pay attention to the humidity in the work area.
50~60% RH is recommended.

3-3 Precautions for the soldering of an LCM

The following procedures should be followed when soldering the LCM:

A. Solder only to the I/O terminal.

B. Use a no leakage soldering iron and pay particular attention to the following:

(1) Conditions for soldering I/O terminals

Temperature at iron tip : 280°C+ 10°C

Soldering time : 3-4 sec/terminal

Type of solder : Eutectic solder (rosin flux filled)

Note: Avoid using flux, because it could penetrate the module and the module may get contaminated during cleaning. Peel off protective film after soldering of the I/O terminals is finished. By following this procedure, the surface contamination, caused by the dispersion of flux while soldering, can be avoided.

(2) Removing the wiring

When a lead wire or a connector to the I/O terminal of the module is to be removed, remove it only after the solder at the connection has sufficiently melted since the I/O terminal is a through hole. If it is forcefully removed, it could cause the terminal to break or peel. The recommended procedure is to use a suction-type solder remover. Caution, do not reheat the I/O terminal more than 3 times.

3-4. Long-term storage

If the correct method of storage is not followed, deterioration of the display material polarizer and oxidation of the I/O terminal plating may make the soldering process difficult. Please comply with the following procedure.

A. Store in the shipping container.

B. If the shipping container is not available, place in anti-static bags and seal the opening

C. Store the modules where they are not subjected to direct sunlight or a fluorescent lamp.

D. Store in a temperature rang of 0°C~35°C with low relative humidity.

3-5. Precautions in use of LCD modules

A. Do not give any external shock.

B. Do not wipe the surface with hard materials.

C. Do not apply excessive force on the surface.

D. Do not expose to direct sunlight or fluorescent light for a long time.

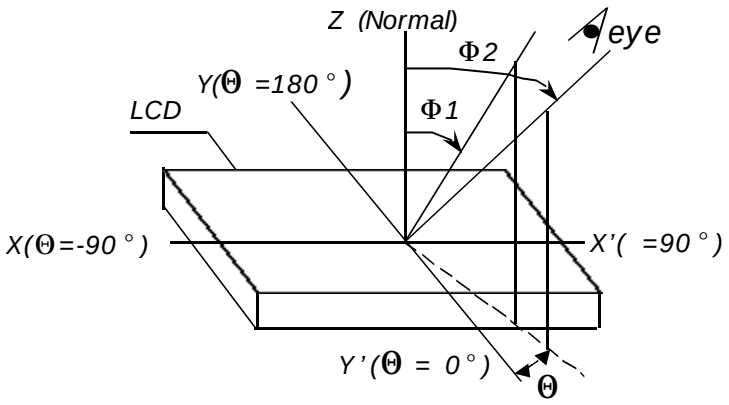
E. Avoid storage in high temperature and high humidity.

F. When storage for a long time at 40°C or higher is required, R/H shall be less than 60%.

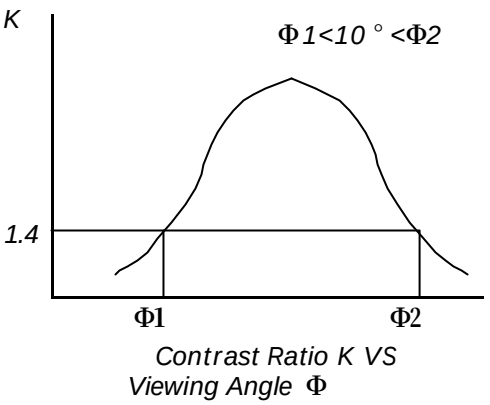
G. Liquid in LCD is hazardous substance. Must not lick, swallow when the liquid is attached to your hands, skin, clothes etc. Wash it out thoroughly.

4. Optical definitions

4.1 Definition of angle Θ and Φ



4.2 Definition of viewing angle Φ1 and Φ2

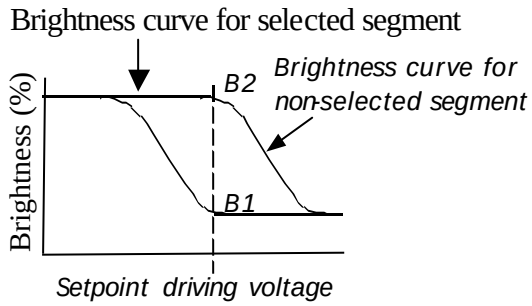


Contrast Ratio K VS Viewing Angle Φ

POSITIVE TYPE

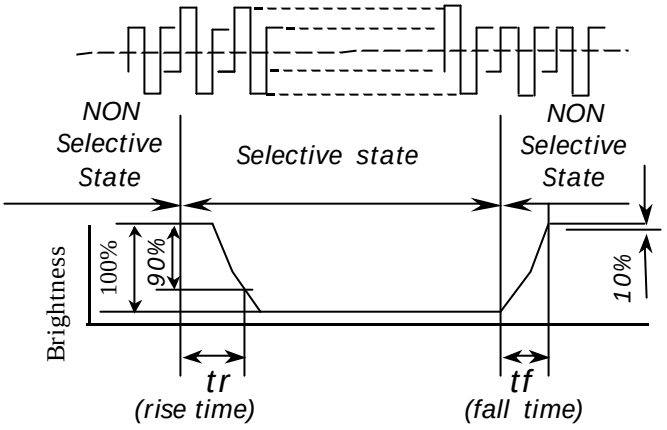
4.3 Definition of contrast "K"

$$K=\frac{\text{Brightness of non-selected segment (B2)}}{\text{Brightness of selected segment (B1)}}$$



POSITIVE TYPE

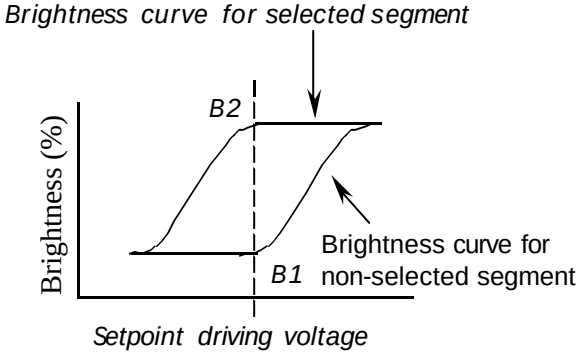
4.4 Definition of optical response



NEGATIVE TYPE

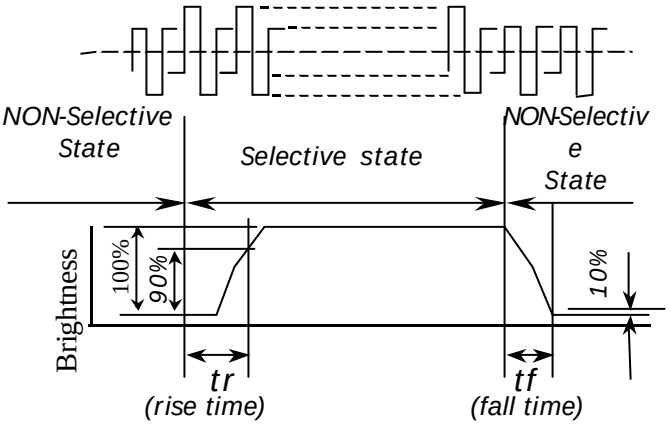
4.5 Definition of contrast "K"

$$K=\frac{\text{Brightness of selected segment (B1)}}{\text{Brightness of non-selected segment (B2)}}$$



NEGATIVE TYPE

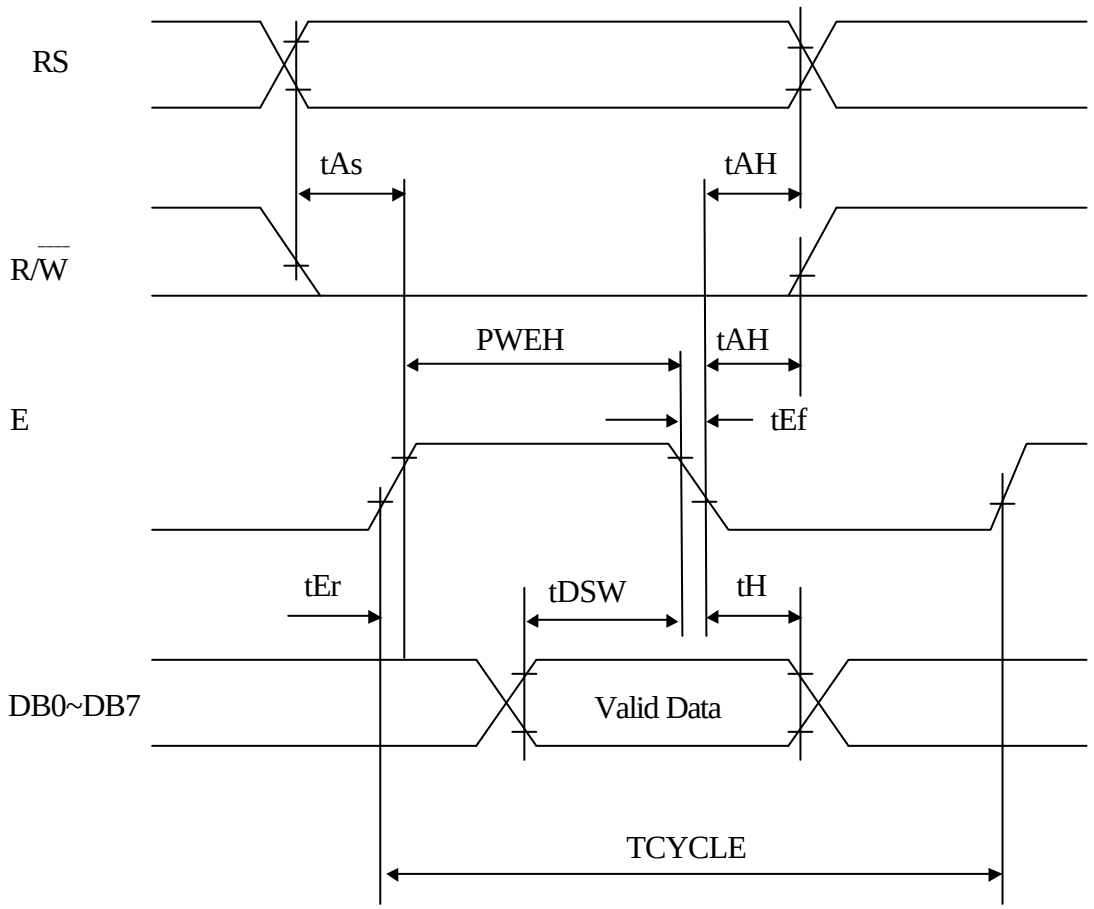
4.6 Definition of optical response



5. Timing characteristics

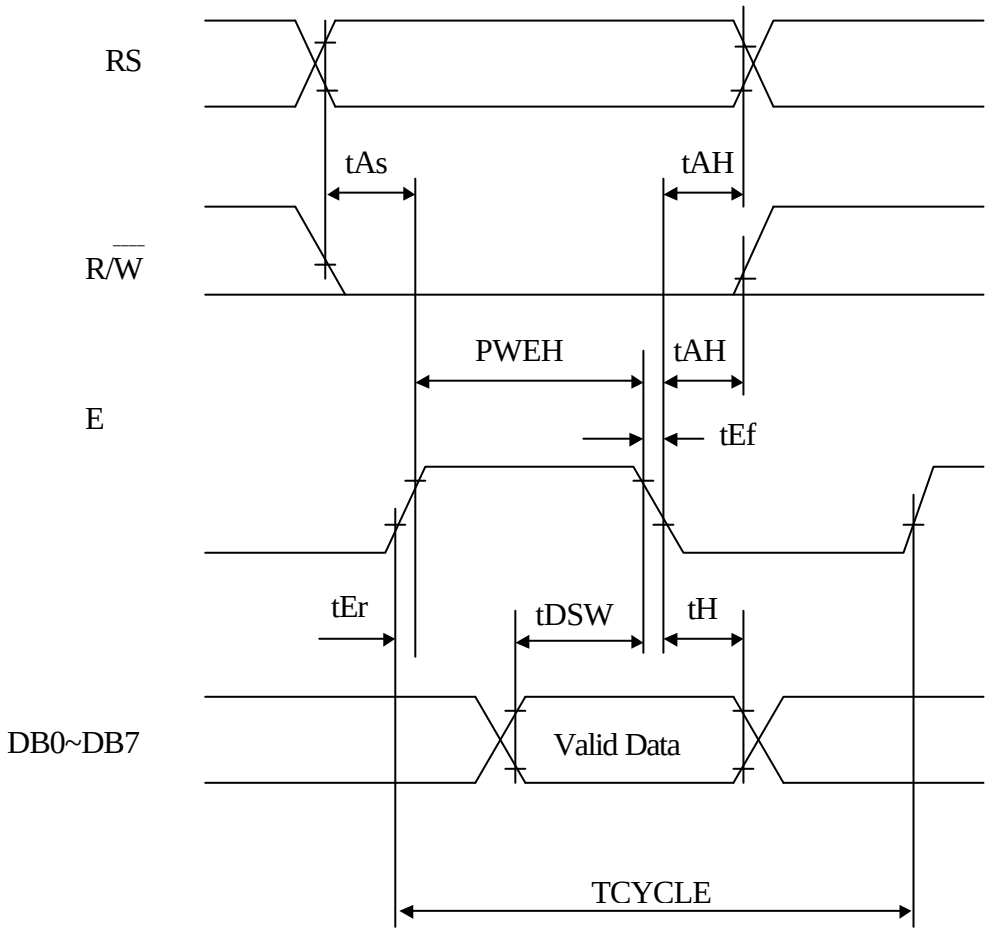
5.1 (1) Write operation (V_{DD}=4.5~5.5V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Enable cycle time	TCYCLE	500	------	------	ns
Enable pulse width	PWEH	230	------	------	ns
Enable rise & fall time	tEr, tEf	------	------	20	ns
Address set-up time	tAs	40	------	------	ns
Address hold time	tAH	10	------	------	ns
Data set-up time	tDSW	60	------	------	ns
Data hold time	^{t}H	10	------	------	ns



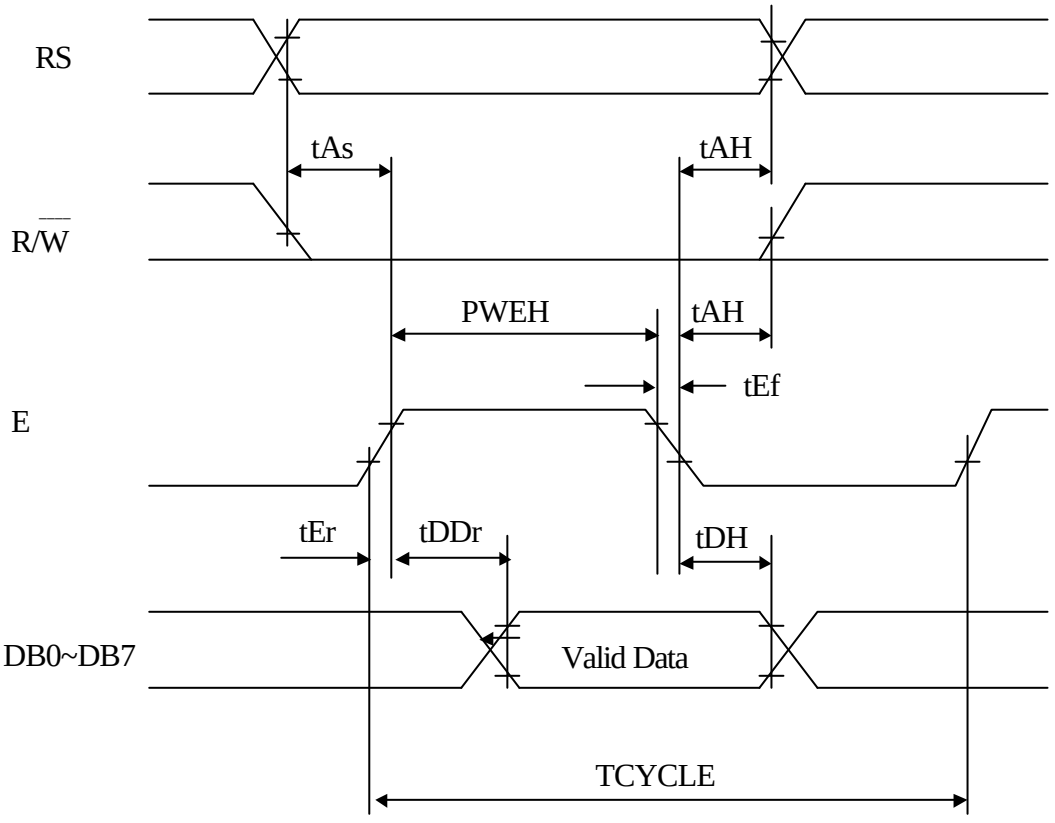
(2) Write operation (V_{DD}=2.7~5.5V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Enable cycle time	TCYCLE	1.0	------	------	μs
Enable pulse width	PWEH	450	------	------	ns
Enable rise & fall time	tEr, tEf	------	------	25	ns
Address set-up time	tAs	60	------	------	ns
Address hold time	tAH	20	------	------	ns
Data set-up time	tDSW	195	------	------	ns
Data hold time	tH	10	------	------	ns



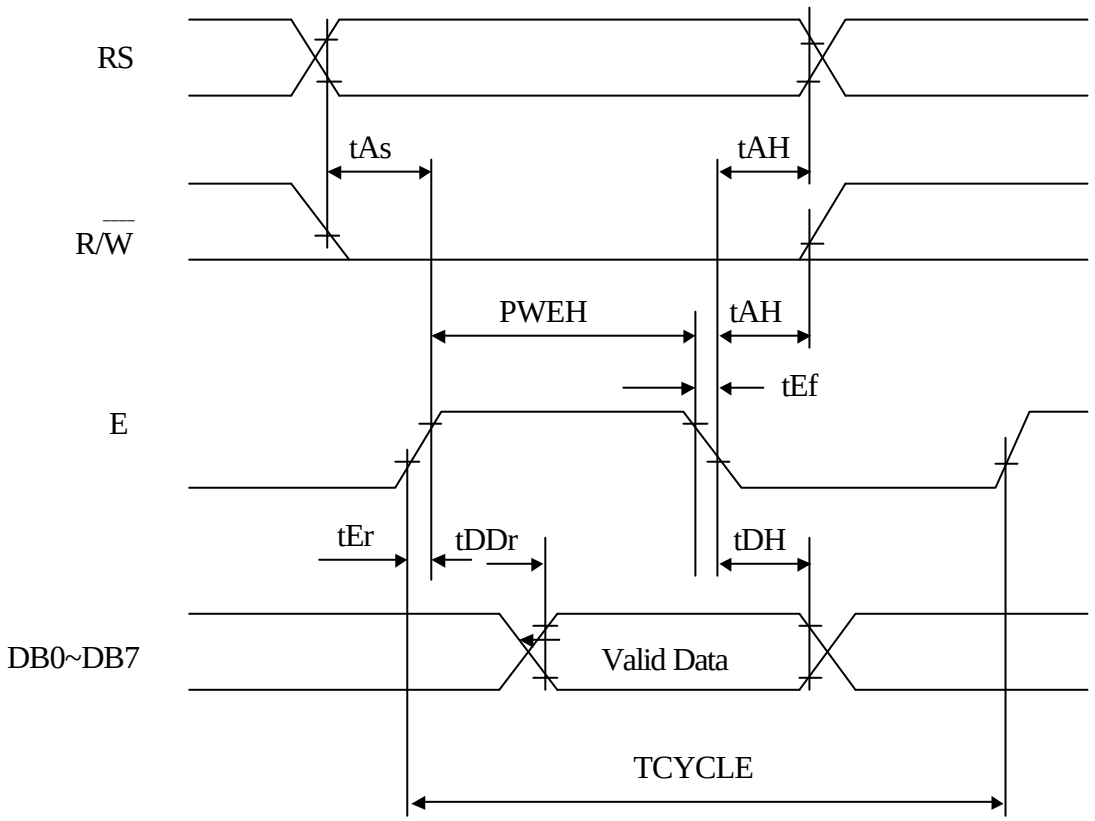
5.2 (1) Read operation (V_{DD}=4.5~5.5V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Enable cycle time	TCYCLE	500	------	------	ns
Enable pulse width	PWEH	230	------	------	ns
Enable rise & fall time	tEr, tEf	------	------	20	ns
Address set-up time	tAs	40	------	------	ns
Address hold time	tAH	10	------	------	ns
Data delay time	tDDr	------	------	160	ns
Data hold time	^{t}DH	5	------	------	ns



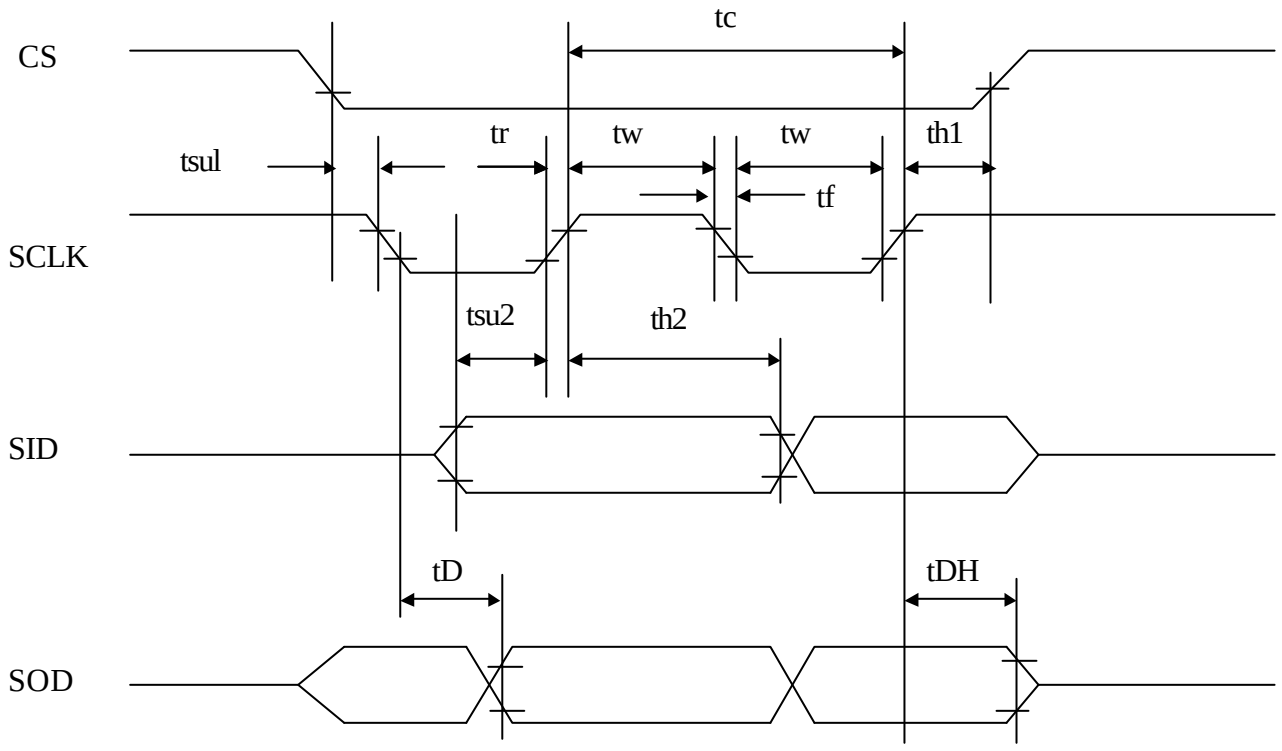
(2) Read operation (V_{DD}=2.7~5.5V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Enable cycle time	TCYCLE	1.0	------	------	μs
Enable pulse width	PWEH	450	------	------	ns
Enable rise & fall time	tEr, tEf	------	------	25	ns
Address set-up time	tAs	60	------	------	ns
Address hold time	tAH	20	------	------	ns
Data delay time	tDDr	------	------	360	ns
Data hold time	^{t}DH	5	------	------	ns



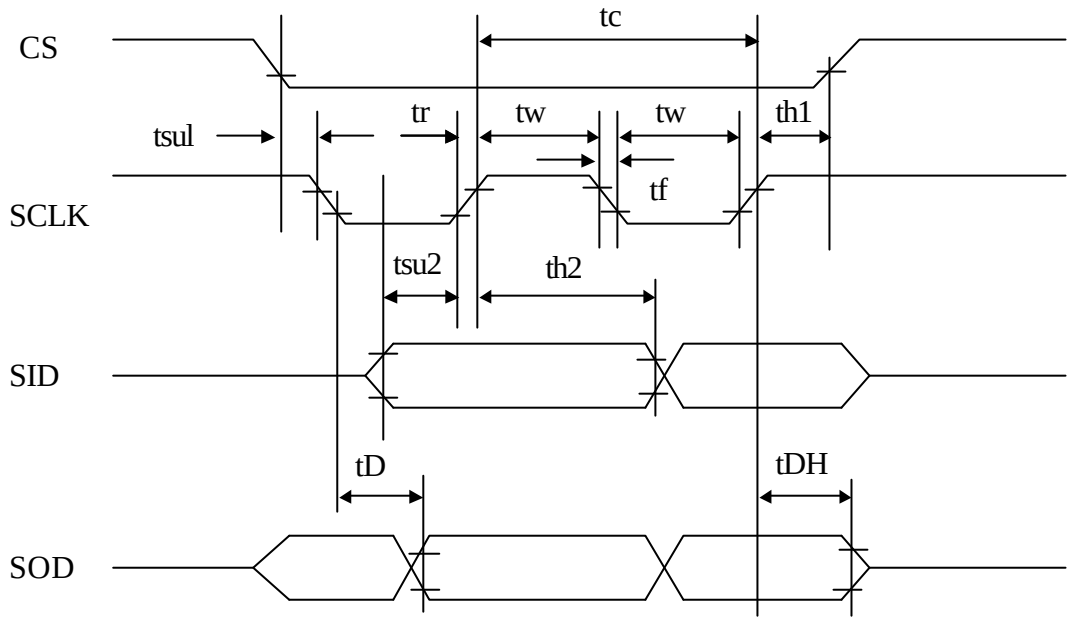
5.3 (1) Serial operation (V_{DD}=4.5~5.5V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Serial clock cycle time	tc	0.5	------	20	μs
Serial clock width	tw	200	------	------	ns
Serial clock rise & fall time	tr, tf	------	------	50	ns
Chip select set-up time	tsu1	60	------	------	ns
Chip select hold time	tH1	20	------	------	ns
Serial input data set-up time	tsu2	100	------	------	ns
Serial input data hold time	tH2	100	------	------	ns
Serial output data delay time	tD	------	------	160	ns
Serial output data hold time	tDH	5	------	------	ns



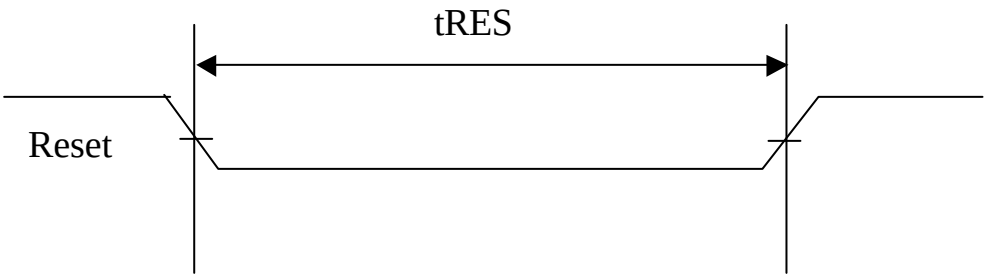
(2) Serial operation (V_{DD}=2.7~5.5V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Serial clock cycle time	tc	1.0	------	20	μs
Serial clock width	tw	400	------	------	ns
Serial clock rise & fall time	tr, tf	------	------	50	ns
Chip select set-up time	tsu1	60	------	------	ns
Chip select hold time	tH1	20	------	------	ns
Serial input data set-up time	tsu2	200	------	------	ns
Serial input data hold time	tH2	200	------	------	ns
Serial output data delay time	tD	------	------	360	ns
Serial output data hold time	tDH	5	------	------	ns



5.4 Reset operation (V_{DD}=2.7~5.5V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Reset low level width	tRES	10	------	------	ms



6. Functional description

6.1 System interface

This chip has three kinds interface type with MPU: serial, 4-bit bus and 8-bit bus. Serial and bus (4-bit/8-bit) is selected by IM input, and 4-bit bus and 8-bit bus is selected by DL bit in the instruction register.

6.2 Register

During read or write operation, two 8-bit registers are used. One is data register (DR), the other is instruction register (IR). The data register (DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. Hence, after MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically. The instruction register (IR) is used only to store instruction code transferred from MPU.MPU cannot use it to read instruction data. To select register, use RS/CS input pin in 4-bit/8-bit bus mode (IM= "High") or RS bit in serial mode (IM="LOW")

RS	$R/\overline{W}$	Operation
0	0	Instruction write operation (MPU writes instruction code into IR)
0	1	Read busy flag (DB7) and address counter (DB0~DB6)
1	0	Data write operation (MPU writes data into DR)
1	1	Data read operation (MPU reads data from DR)

6.3 Busy flag (BF)

When BF= ”High ”, it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS= Low and R/W= High (Read Instruction Operation),through DB7 port. Before executing the next instruction, be sure that BF is not High.

6.4 Address counter (AC)

Address counter (AC) stores DDRAM/CGRAM address, transferred from IR. After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1. When RS= ”Low” and R/$\overline{W}$= “High”, AC can be read through DB0~DB6 ports.

6.5 Display data RAM (DDRAM)

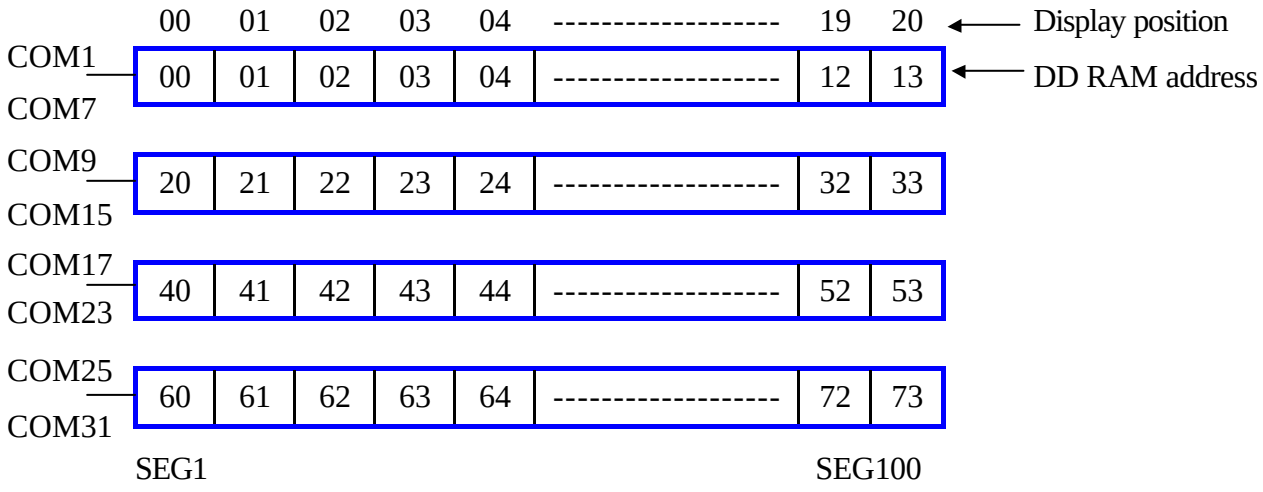
DDRAM stores display data of maximum 80*8 bits (80 characters). DDRAM address is set in the address counter (AC) as a hexadecimal number.

MSB LSB

AC6	AC5	AC4	AC3	AC2	AC1	AC0

(DDRAM Address)

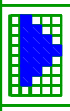
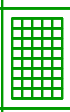
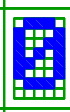
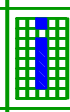
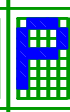
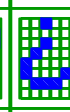
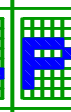
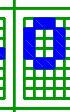
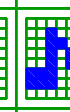
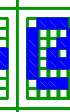
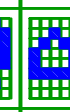
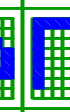
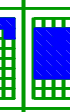
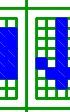
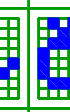
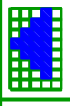
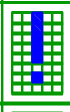
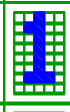
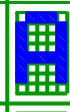
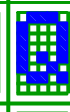
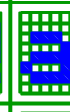
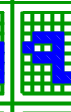
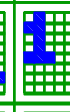
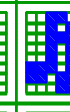
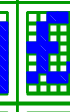
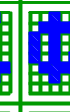
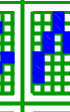
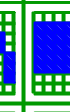
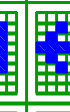
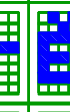
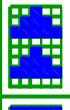
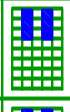
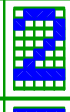
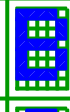
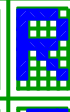
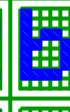
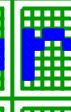
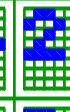
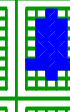
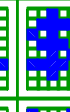
4 line display with 5-dot font, the address range of DDRAM is 00H~13H, 20H~33H, 40H~53H, 60H~73H.



6.6 Character generator ROM(CG ROM)

CGROM has 5*8-dot 240 character pattern

CGROM Character Code Table

Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	(2)															
LLHL	(3)															
LLHH	(4)															
LHLL	(5)															
LHLH	(6)															
LHHL	(7)															
LHHH	(8)															
HLLL	(1)															
HLLH	(2)															
HLHL	(3)															
HLHH	(4)															
HHLL	(5)															
HHLH	(6)															
HHHL	(7)															
HHHH	(8)															

6.7 CHARACTER GENERATOR FOR (CG RAM)

CGRAM has up to 5*8-dot 8 characters. By writing font data to CGRAM, user defined character can be used.

(a) In the case of 5*7 dots character patterns

Character codes (DD RAM Data)		CG RAM Address		Character Patterns (CG RAM Data)		
7 6 5 4 3 2 1 0		5 4 3	2 1 0	7 6 5	4 3 2 1 0	
0 0 0 0 * 0 0 0		0 0 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0	B1B0＊	1 1 1 1 1 1 0 0 0 1 1 0 0 0 1 1 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 1 1 1 0	Character Pattern Example(1)
0 0 0 0 * 0 0 1		0 0 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0	B1B0＊	0 1 1 1 1 1 0 0 0 0 1 0 0 0 0 0 1 1 1 0 0 0 0 0 1 0 0 0 0 1 1 1 1 1 0	Character Pattern Example(2)
			0 0 0 0 0 1	B1B0＊	1 1 1 1 1 0 0 1 0 0	
0 0 0 0 * 1 1 1		1 1 1	0 1 1 1 0 0 1 0 1 1 1 0	B1B0＊	0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0	

Note 1: When BE (Blink Enable bit)="High", blink is controlled by B1 and B0 bit.

In displaying 5-dot font width, when B1-1, enable dots of P0~P4 will blink, and when B1="0" and B0="1", enable dots in P4 will blink, when B1="0" and B0="0", blink will not happen.

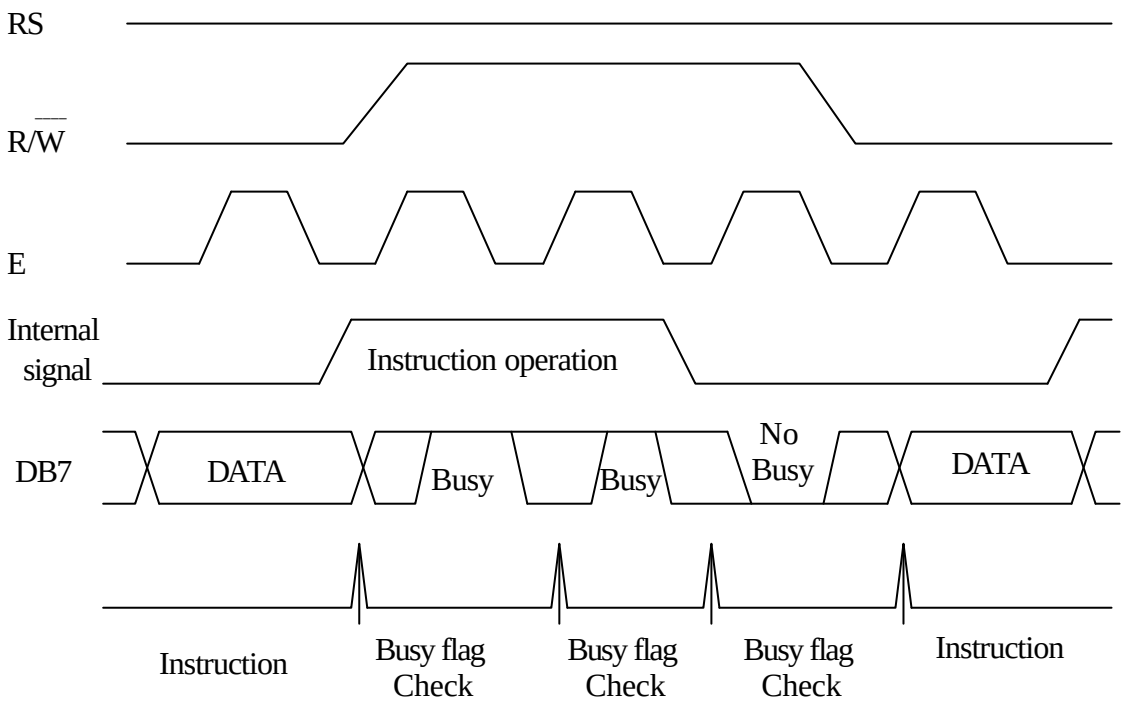
2. "＊": Don't care

6.8 Interfacing with MPU

The VLSI can transfer data in bus mode (4-bit or 8-bit) or serial mode with MPU. Hence, both types of 4 or 8-bit MPU can be used. In case of 4-bit bus mode, transfer is performed by twice to transfer 1 byte data.

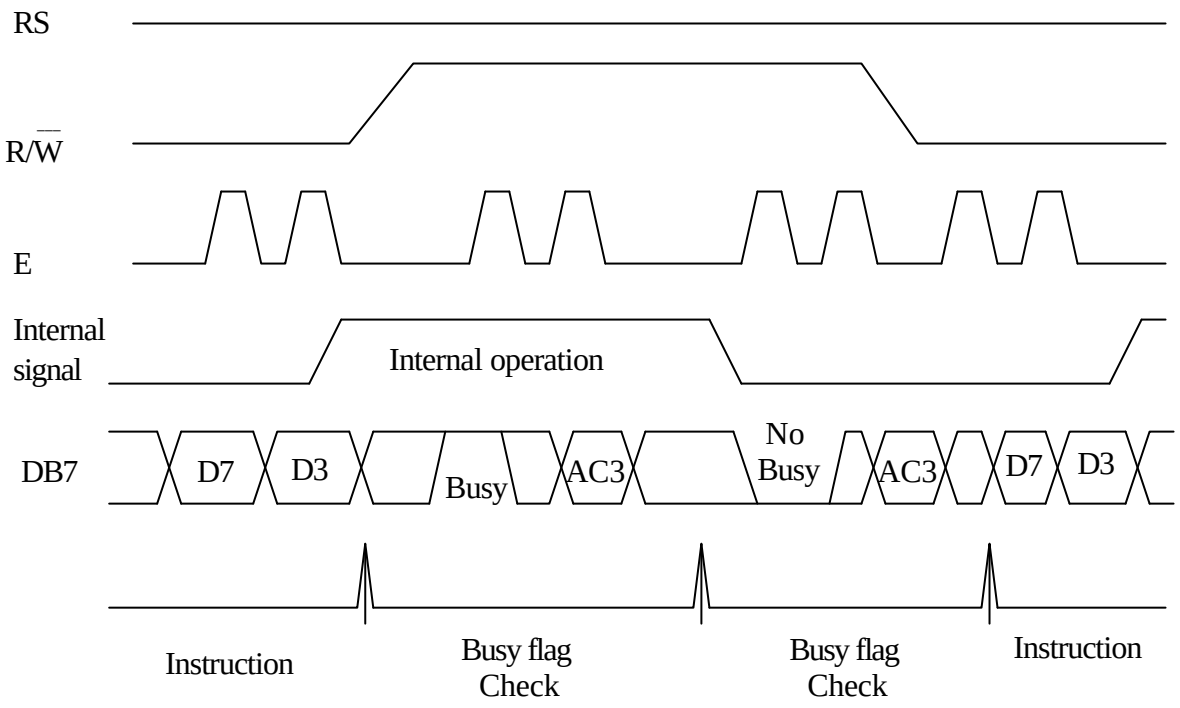
(1) Interface with 8-bits MPU

IF 8-bits MPU is used, The VLSI can connect directly with that. In this case, port E, RS, R/$\overline{W}$ and DB0 to DB7 need to interface each other.



(2). Interface with 4-bits MPU

If 4-bits MPU is used, The VLSI can connect directly with that. In this case, port E, RS, R/$\overline{W}$ and DB4 to DB7 need to interface each other. The transfer is performed by twice.



(3) Interface with MPU in Serial Mode

When IM port input is “LOW”, serial interface mode is started. At this time, all three ports, SCLK (synchronizing transfer clock), SID (serial input data), and SOD (serial output data), are used. IF the VISI is be used with other chips, chip select port (cs) be used By setting CS to “LOW”, The VLSI can receive SCLK input, If CS is set to “HIGH”, The VISI reset the internal transfer counter.

Before transfer real data, start byte has to be transferred. It is composed of succeeding 5 ”HIGH” bits, read write control bit ($R/\overline{W}$), register selection bit (RS), and end bit that indicates the end of start byte. Whenever succeeding 5 ”HIGH”bits are detected by The VLSI, it resets serial transfer counter and prepares to receive next information.

The next input data are register selection bit which determine which register is to be used, and read write control bit that determine the direction of data, then end bit is transferred, which must have “Low” value to show the end of start byte.

1. Write Operation ($R/\overline{W}$ =0)

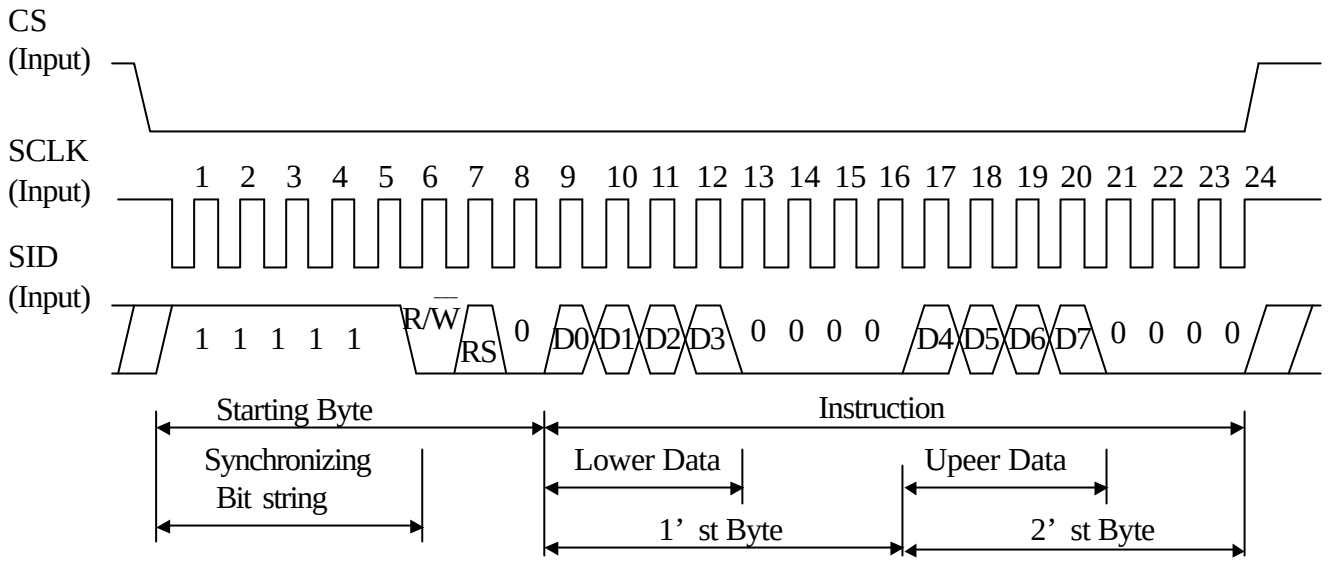
After start byte is transferred from MPU to The VLSI, 8-bit data is transferred which is divided into 2 bytes, each byte has 4-bit’s real data and 4 bit’s partition token data.

2. Read Operation ($R/\overline{W}$=1)

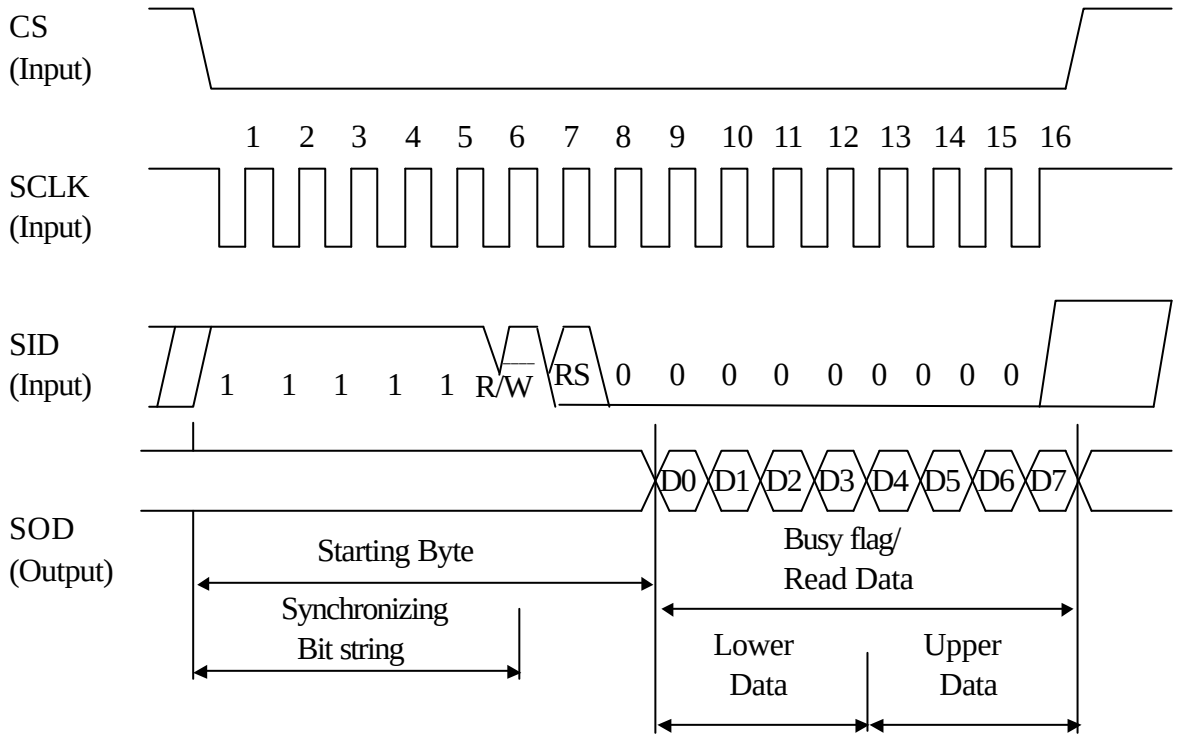
After start byte is transferred to The VLSI, MPU can receive 8-bit data through the SOD port at a time from the LSB. Wait time is needed ot insert between start byte and data reading, as internal reading from RAM requires some delay.

Continuous data reading is possible such as serial write operation. It also needs only one start bytes, only if some delay between reading operation of each byte is inserted. During the reading operation, The VLSI observes succeeding 5”High” from MPU. If detected, The VLSI restarts serial operation at once and prepares to receive RS bit, So in continuous reading operation, SID port must be “Low”.

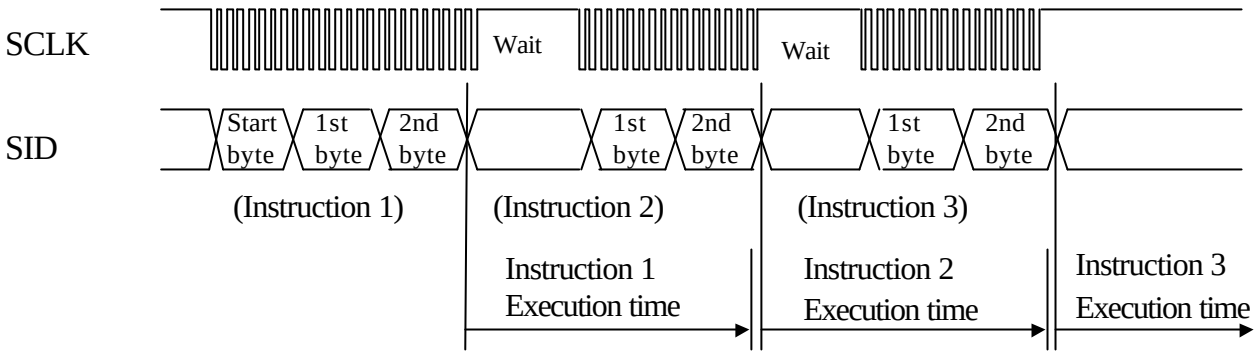
(a) Serial Write Operation



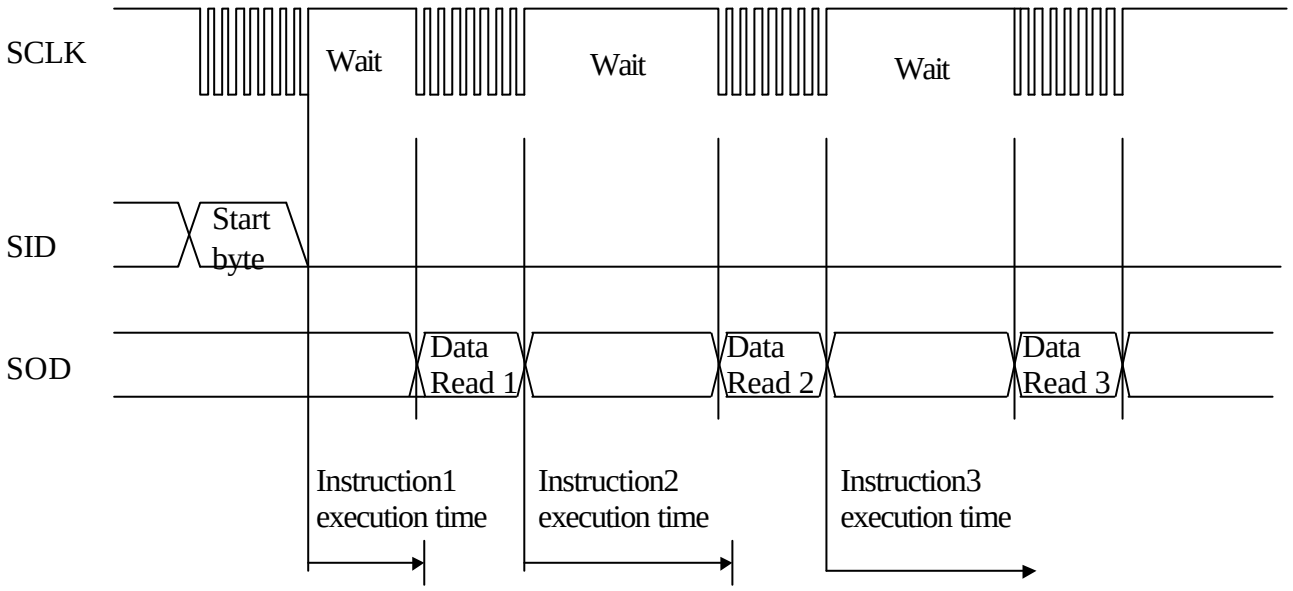
(b) Serial Read Operation



(c) Continuous Write Operation



(d) Continuous Read Operation



6.9 Instruction

To overcome the speed difference between internal clock of The VLSI and MPU clock, The VLSI performs internal operation by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus.

Instruction can be divided largely four kinds.

(1) The VLSI function set instructions.

(2) Address set instruction to internal RAM.

(3) Data transfer instructions with internal RAM.

(4) Others.

The address of internal RAM is automatically increased or decreased by 1.

＊Note：

During internal operation, Bus Flag (DB7) is read High. Busy Flag check must precede the next instruction.

When an MPU program with Busy Flag (DB7) checking is made, 1/2 fosc (is necessary) for executing the next instruction by the falling edge of the “E” signal after the Busy Flag (DB7) goes to “Low”

Instruction	RE	CODE										Description	Execution time (MAX.) (fcp=270KKKHz)
		RS	R/$\overline{W}$ ($\overline{WR}$)	D7	D6	D5	D4	D3	D2	D1	D0		
Clear Display	*	0	0	0	0	0	0	0	0	0	1	Write “20H” to DDRAM. and set DDRAM address to “00H” from AC.	1.53ms
Return Home	0	0	0	0	0	0	0	0	0	1	*	Set DDRAM address to “00H” from AC and return cursor to its original position. If shifted. The contents of DDRAM are not changed.	1.53ms
Power Down Mode	1	0	0	0	0	0	0	0	0	1	PD	Set power down mode bit. PD=”1”:power down mode set. PD=”0”:power down mode disable.	39μs
Entry Mode Set	0	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction. I/D=”1” ：increment I/D=”0”: decrement. and display shift enable bit. S=”1”:make display shift of the enabled lines by the DS4~DS1 bits in the Shift Enable instruction. S=”0”:display shift disable.	39μs
	1	0	0	0	0	0	0	0	1	1	BID	Segment bi-direction BID=”1”：Seg100 → Seg 1 BID=”0”：Seg1 → Seg100.	39μs
Display On/Off Control	0	0	0	0	0	0	0	1	D	C	B	Set display/blink on/off, D=”1” ：display on, D=”0” ：display off, C=”1” ：cursor on, c=”0” ：cursor off, B=”1” ：blink on, B=”0” ：blink off,	39μs
Extended Function Set	1	0	0	0	0	0	0	1	0	B/$\overline{W}$	1	5-dot font width, and 4-line display mode. B/$\overline{W}$=”1” ：black/white inverting of cursor enable. B/$\overline{W}$=”0” ：black/white inverting of cursor disable.	39μs

Instruction	RE	CODE										Description	Execution Time (MAX.) (fcp=270KHz)
		RS	R/ W (WR)	D7	D6	D5	D4	D3	D2	D1	D0		
Cursor or Display Shift	0	0	0	0	0	0	1	S/C	R/L	*	*	Cursor or display shift. S/C="1" : Display shift, S/C="0" : Cursor shift, R/l="1" : shift to right, R/L="0" : shift to left.	39 μs
Shift Enable	1	0	0	0	0	0	1	DS4	DS3	DS2	DS1	(when DH="1") in function set. Determine the line for display shift. DS1="1/0" : 1st line display shift enable/disable, DS2="1/0" : 2nd line display shift enable/disable, DS3="1/0" : 3rd line display shift enable/disable, DS4="1/0" : 4th line display shift enable/disable.	39 μs
Scroll Enable	1	0	0	0	0	0	1	HS4	HS3	HS2	HS1	(when DH="0") in function set. Determine the line for horizontal smooth scroll. HS1="1/0" : 1st line dot scroll enable/disable, HS2="1/0" : 2nd line dot scroll enable/disable, HS3="1/0" : 3rd line dot scroll enable/disable, HS4="1/0" : 4th line dot scroll enable/disable,	39 μs
Function Set	0	0	0	0	0	1	DL	*	RE (0)	DH	REV	Set interface data length (DL="1/0" ; 8-bit/4-bit), Extension register, RE(0),shift/scroll enable DH="1/0" : display shift enable/dot scroll enable. reverse bit REV="1/0" : reverse display/normal display.	39 μs
	1	0	0	0	0	1	DL	*	RE (1)	BE	0	Set DL.RE("1") and CGRAM blink enable (BE) BE="1/0" : CGRAM Blink enable/ disable.	
Set CGRAM Address	0	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39 μs

Instruction	RE	CODE										Description	Execution Time (MAX.) (fcp=270KHz)
		RS	R/$\overline{W}$ ($\overline{WR}$)	D7	D6	D5	D4	D3	D2	D1	D0		
Set DDRAM Address	0	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39μs
Set Scroll Quantity	1	0	0	1	*	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Set the quantity of horizontal dot scroll.	39μs
Read busy flag and address	*	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Can be known whether during internal operation or not by reading BF. The contents of address counter can also be read. BF="1"：busy state, BF="0"：ready state.	0μs
Write data	*	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM(DDRAM/CGRAM)	43μs
Read data	*	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM(DDRAM/CGRAM)	43μs

Note：

1.When an MPU program with Busy Flag (DB7)

Checking is made, 1/2 fosc (is necessary) for executing the next instruction by the "E" signal after the Busy Flag (DB7) goes to "Low"

2. "*"：Don't care

3. The module is no cursor.

(a) Clear display

	RS	R/$\overline{W}$ / $\overline{WR}$	DB7						DB0
Instruction code	0	0	0	0	0	0	0	0	1

Clear all the display by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, hence, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D="1")

(b) Return home

	RS	R/$\overline{W}$ / $\overline{WR}$	DB7							DB0	
Instruction code	0	0	0	0	0	0	0	0	1	*	*：Invalid

Return home is cursor return home instruction.
Set DDRAM address to "00H" into the address counter.
Return cursor to its original site and return display to its original status, if shifted.
Contents of DDRAM does not change.

(c) Power down mode set：(RE=1)

	RS	R/$\overline{W}$ / $\overline{WR}$	DB7							DB0
Instruction code	1	0	0	0	0	0	0	0	1	PD

Power down mode enable bit set instruction.
PD= "High", it makes The VLSI suppress current consumption except the current needed for data storage by executing next three functions.

1. Make the output value of all the COM/SEG ports V_{DD}.
2. Make the COM/SEG output value of extension driver V_{DD} by setting D output to "High" and M output to "Low".
3. Disable voltage converter to remove the current though the divide resistor of power supply.

This instruction can be used as power sleep mode.
When PD= "Low", power down mode becomes disabled.

(d) Entry mode set

1.(RE=0)

	RS	$\overline{R/W}$ / $\overline{WR}$	DB7						DB0
Instruction code	0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of display. ID：Increment/decrement of DDRAM address (blink). When I/D= ”High” , blink moves to right and DDRAM address is decreased by 1.When I/D= “Low” , blink moves to left and DDRAM address is decreased by 1. ＊CGRAM operates the same as DDRAM, when read from or write to CGRAM. When S= “High”, after DDRAM write, the display of enabled line by DS1~DS4 bits in the shift Enable instruction is shifted to the right (I/D=”0”) or to the left (I/D=”1”). When S= ”Low”, or DDRAM read, or CGRAM read/write operation, shift or display like this function is not performed.

2. (RE=1)

	RS	$\overline{R/W}$ / $\overline{WR}$	DB7						DB0
Instruction code	0	0	0	0	0	0	0	1	1	BID

Set the data shift direction of segment in the application set.

BID: Data shift Direction of Segment. When BID= ”Low”, segment data shift direction is set to reverse order from SEG1 to SEG100. When BID =”High”, segment data shift direction is set to normal from SEG100 to SEG1. By using this instruction, the efficiency of application broad area can be raised.＊The BID setting instruction is recommended to be set at the same time level of function set instruction.＊DB1 bit must be set to 1.

(e) Display ON/OFF control (RE=0)

	RS	R/$\overline{W}$ / $\overline{WR}$	DB7							DB0
Instruction code	0	0	0	0	0	0	1	D	*	B

Control display /blink ON/OFF 1 bit register.

D: Display ON/OFF control bit.

When D= "High", entire display is turned on.

When D= "Low", display is turned off, but display data is remained in DDRAM.

B: Blink ON/OFF control bit.

When B= "High", blink is on, that performs alternate between all the high data and display character length position. If fosc has 270 KHZ frequency, blinking has 370 ms interval.

When B= "Low", blink is off.

(f) Extended function set.(RE=1)

	RS	R/$\overline{W}$ / $\overline{WR}$	DB7							DB0
Instruction code	0	0	0	0	0	0	1	0	B/$\overline{W}$	1

5-dot font width and 4 line display mode is set.

B/$\overline{W}$: Black/White Inversion enable bit

When B/$\overline{W}$= "High" , black/white inversion at the display address position is set. In this case B bit of display ON/OFF control instruction becomes don't care condition. If fosc has frequency of 270 KHZ. inversion has 370 ms intervals.

(g) Cursor or display shift (RE=0)

	RS	$\overline{R/W}$ / $\overline{WR}$	DB7							DB0
Instruction code	0	0	0	0	0	1	S/C	R/L	*	*

Shift right/left cursor position or display, with out writing or reading of display data, this instruction is used to correct or search display data.

＊Note：that display shift is performed simultaneously in all the line enabled by DS1~DS4 in the Shift Enable instruction. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed. During low power consumption mode, display shift may not be performed normally.

S/C	R/L	Functions
0	0	Shift cursor to the lift, ADDRESS COUNTER is decreased by 1.
0	1	Shift cursor to the right, ADDRESS COUNTER is increased by 1.
1	0	Shift all the display to left, cursor moves according to the display.
1	1	Shift all the display to right, cursor moves according to the display.

Shift patterns according to S/C and R/L bits

(h) Shift/scroll enable (RE=1)

1.(DH=0)

	RS	R/W / WR	DB7							DB0
Instruction code	0	0	0	0	0	1	HS4	HS3	HS2	HS1

HS：Horizontal scroll per Line Enable

This instruction makes valid dot shift by a display line unit, HS1, HS2, HS3 and HS4 indicate each line to be dot scrolled, and each scroll is performed individually in each line.

2.(DH=1)

	RS	R/W / WR	DB7							DB0
Instruction code	0	0	0	0	0	1	DS4	DS3	DS2	DS1

DS：Display shift per Line Enable

This instruction selects shifting line to be shifted according to each line mode in display shift right/left instruction. DS1, DS2,DS3 and DS4 indicate each line to be shifted, and each shift is performed individually in each line. If all the DS bits (DS1 to DS4) are set to “Low” (disable), no display is shifted.

Enable bit	Enable common signals During shift	Description
HS1/DS1	COM1~DOM7	The part of display line that corresponds to enabled common signal can be shifted.
HS2/DS2	COM9~DOM15	
HS3/DS3	COM17~DOM23	
HS4/DS4	COM25~DOM31	

Relationship between DS and COM signal

(i) Function set

1.(RE=0)

	RS	R/W / WR	DB7							DB0
Instruction code	0	0	0	0	1	DL	*	RE	DH	REV

DL：Interface data length control bit

When DL= ”High” , it means 8-bit bus mode with MPU. When DL=

“Low”, it means 4-bit bus mode with MPU, Hence, DL is a signal to

select 8-bit or 4-bit bus mode. In 4-bit bus mode, In 4-bit bus mode, it is

required to transfer 4-bit data twice.

RE：Extended function registers enable bit

At this instruction, RE must be “Low”.

DH：Display shift enable selection bit

When DH= ”High”, enable display shift per line. When DH= ”Low”,

enable smooth dot scroll.

REV：Reverse enable bit

When REV= ”High”, all the display data are reversed.1.e., all the white dots become black and black dots become white. When REV= ”Low”, the display mode set normal display.

.2. (RE=1)

	RS	R/W / WR	DB7							DB0
Instruction code	0	0	0	0	1	DL	*	RE	BE	0

DL：Interface data length control bit

When DL= ”High”, it means 8-bit bus mode with MPU. When DL= ”Low”, it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode. In 4-bit bus mode, it is required to transfer 4-bit data twice.

RE：Extended function registers enable bit

When RE= “High”, extended function set registers, BID bit, HS/DS bit of shift/scroll enable instruction and BE bits of function set register can be accessed.

BE：CGRAM data blink enable bit

BE= “High”, makes user font of CGRAM blinking. The quantity or blink is assigned the highest 2 bits of CGRAM.

(j) Set CGRAM address (RE=0)

	RS	R/W / WR	DB7							DB0
Instruction code	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC. This instruction makes CGRAM data available from MPU.

(k) Set DDRAM address (RE=0)

	RS	R/$\overline{W}$ / $\overline{WR}$	DB7							DB0
Instruction code	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC. This instruction makes DDRAM data available from MPU.DDRAM address is from “00H” to “13H” in the 1st line, from “20H” to “33H” in the 2nd line , from “40H” to “53H” in the 3rd line and from “60H” to 73”H” in the 4th line.

(l) set scroll quantity (RE=1)

	RS	R/$\overline{W}$ / $\overline{WR}$	DB7							DB0
Instruction code	0	0	1	*	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0

Seting SQ5 to SQ0, horizontal scroll quantity can be controlled in dot units. In this case of The VLSI can show hidden areas of DDRAM by executing smooth scroll from 1 to 48 dots.

SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	FUNCTON
0	0	0	0	0	0	No shift
0	0	0	0	0	1	Shift left by 1-dot
0	0	0	0	1	0	Shift left by 2-dot
:	:	:	:	:	:	:
1	1	*	*	*	*	Shift left by 48-dot

(m) Read busy flag & address

	RS	$\overline{R/W}$ / $\overline{WR}$	DB7							DB0
Instruction code	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether The VLSI is in internal operation or not. If the resultant BF is High, the internal operation is in progress and you have to wait until BF to be Low, which by then the next instruction can be performed. In this instruction the value of address counter can also be read.

(n) Write data to RAM

	$\overline{R/W}$ / $\overline{WR}$	RS	DB7							DB0
Instruction code	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Write binary 8-bit data to DDRAM/CGRAM/. The selection of RAM from DDRAM, CGRAM, is set by the previous address set instruction: DDRAM address set, CGRAM address set, RAM set instruction can also determines the AC direction to RAM. After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

(o) Read data from RAM

	RS	$\overline{R/W}$ / $\overline{WR}$	DB7							DB0
Instruction code	1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM. The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, as the direction of AC is not determined. If RAM data is read several times without RAM address set instruction before read operation, the correct RAM data can be obtained from the second, but the first data would be incorrect, as there is no time margin to transfer RAM data. In DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction: it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly

In case of RAM writer operation, AC is increased/decreased by 1 as in read operation after this. In this time, AC indicates the next address position, but the previous data can only be read instruction.

6.10 Initializing

(1)Initializing by Internal Reset Circuit

. When the power is turned on, The VLSI is initialized automatically by power on

reset circuit. During the initialization, the following instructions are executed, and

BF (Busy flag) is kept：High"(busy state) to the end of initialization.

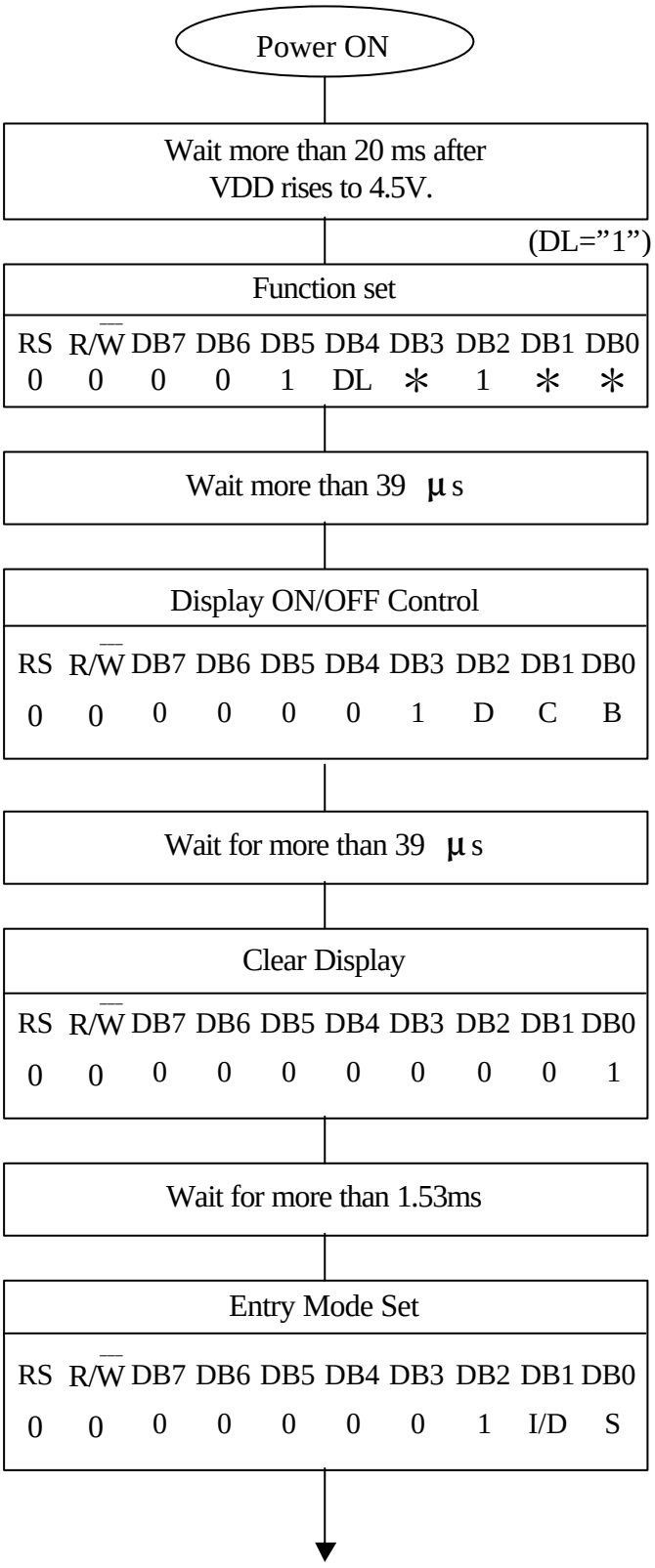
1. Display clear instruction
   Write "20H" to all DDRAM.
2. Set functions instruction
   DL=1：8-bit bus mode.
   RE=0：Extension register display.
   BE=0：CGRAM blink OFF.
   DH=0：Horizontal scroll enable.
   REV=0：Normal display (not reversed display).
3. Control display ON/OFF instruction
   D=0：Display OFF.
   C=0：Cursor OFF.
   B=0：Blink OFF.
4. Set Entry Mode instruction
   I/D=1：Increment by 1.
   S=0：No entire display shift.
   BID=1：Normal direction segment port.
5. Enable shift instruction
   HS=0000：Scroll per line display.
   DS=0000：Shift per line display.
6. Set scroll Quantity instruction
   SQ=0000：Not scroll.

(2) Initializing by Hardware RESET input

When RESET pin= "Low", The VLSI can be initialized like the case of power on reset. During the power on reset operation, this pin is ignored.

(3) Initializing by instruction

1. 8-bit interface mode



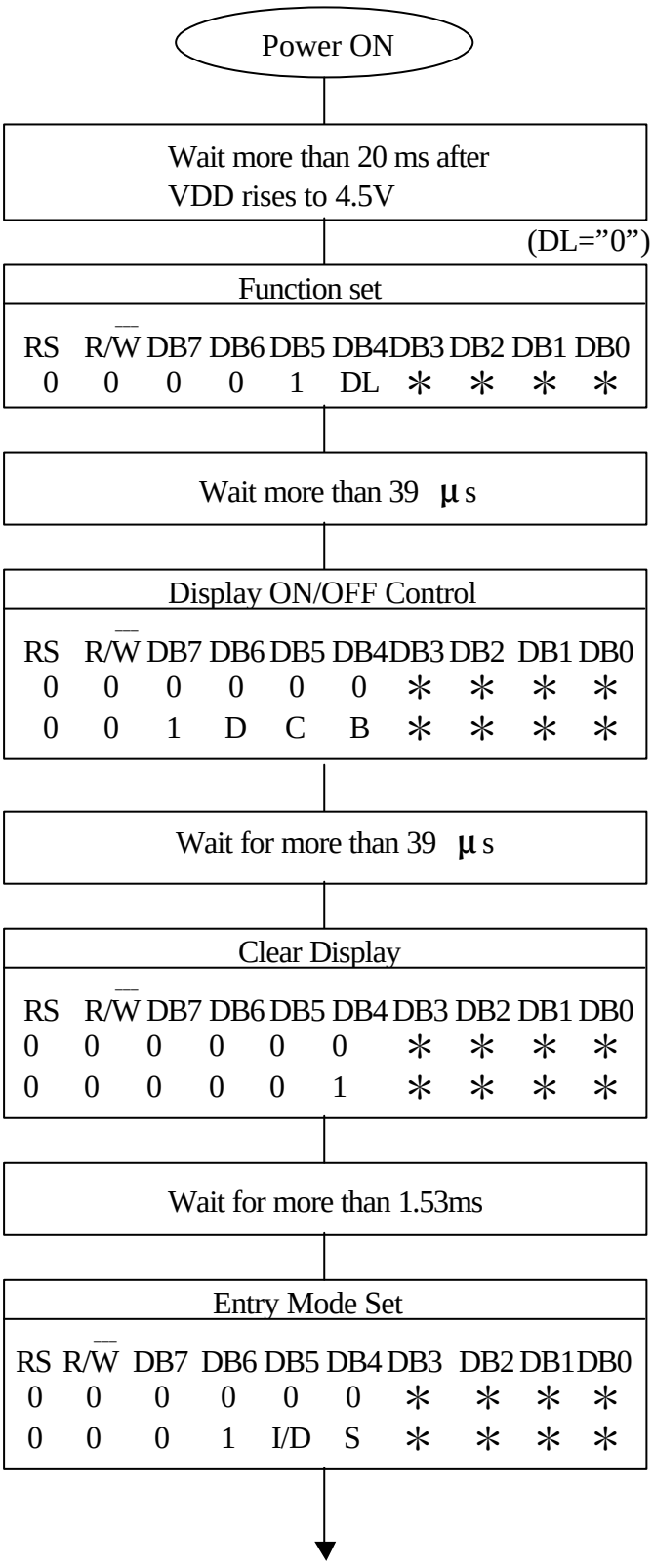
Condition: 270KHz

DL	0	4-bit interface
	1	8-bit interface

B	0	Display off
	1	Display on
C	0	Cursor off
	1	Cursor on
D	0	Blink off
	1	Blink on

I/D	0	Decrement mode
	1	Increment mode
S	0	Entire shift off
	1	Entire shift on

2. 4-bit interface mode



Condition: 270KHz

DL	0	4-bit interface
	1	8-bit interface

B	0	Display off
	1	Display on
C	0	Cursor off
	1	Cursor on
D	0	Blink off
	1	Blink on

I/D	0	Decrement mode
	1	Increment mode
S	0	Entire shift off
	1	Entire shift on

7. Quality and reliability

7-1 Test condition

Test should be conducted under the following conditions:

Ambient temperature: 25±5°C

Humidity :60±20% RH

7-2 Sampling plan

Sampling method shall be in accordance with MIL-STD-105D, inspection level II, normal inspection, and single sampling plan tables for normal tightened, and reduced inspection.

7-3 Acceptable quality level

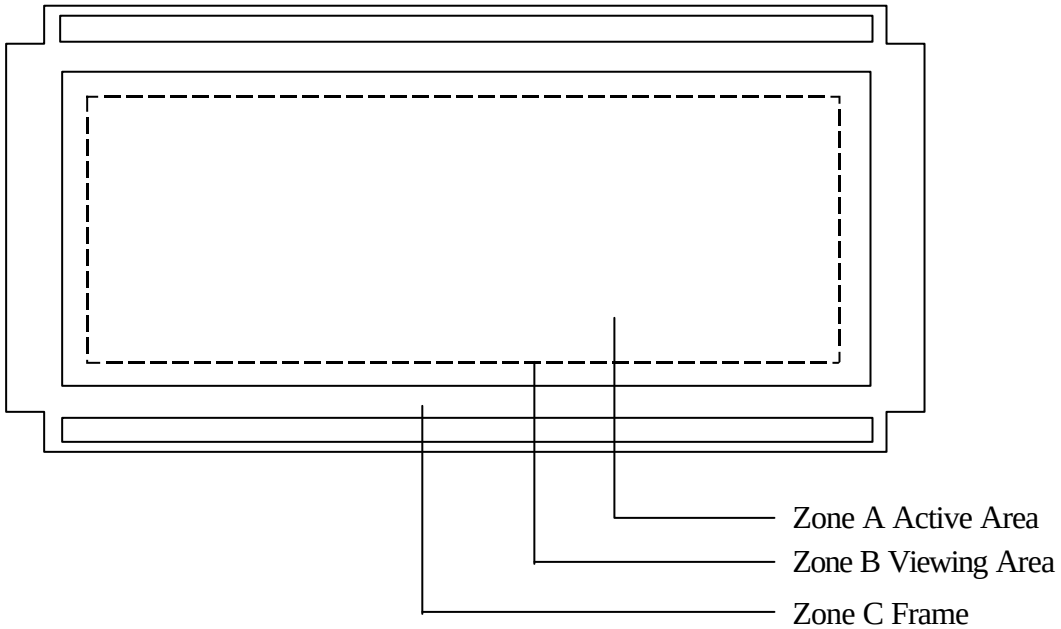
A major defect is a defect that could result in failure or materially reduce that the usability of the unit of product for its intended purpose.

A minor defect is one that does not materially reduce the usability of the unit of product for its intended purpose or is a departure from established standards having no significant bearing on the effective use or operation of the unit.

7-4 Appearance

Appearance test is to be conducted by human eyes at approximately 30 cm distance from LCD module under the single fluorescent light.

The inspection area of LCD panel shall be within the range of following limits.



7-5 Inspection quality criteria

ITME	DESCRIPTION OF DEFECTS			Class of defects	Acceptable level (%)
FUNCTION	Short circuit or Pattern cut			Major	0.65
DIMENSION	Deviation from drawings			Major	2.5
BLACK SPOTS	Ave. dia. D	area A	area B	Minor	2.5
	D ≦ 0.2	disregard			
	0.2 < D ≦ 0.3	3	4		
	0.3 < D ≦ 0.4	2	3		
	0.4 < D	0	1		
BLACK LINES	Width W, Length L	A	B	Minor	2.5
	W ≦ 0.03	disregard			
	0.03 < W ≦ 0.05	3	4		
	0.05 < W ≦ 0.07, L ≦ 3.0	1	1		
	See line criteria				
BUBBLES IN POLARIZER	Average diameter D 0.2 < D < 0.5 mm for N = 4 , D > 0.5 for N =1			Minor	2.5
COLOR UNIFORMITY	Rainbow color or Newton ring.			Minor	2.5
GLASS SCRATCHES	Obvious visible damage.			Minor	2.5
VIEWING ANGLE	See note 2			Minor	2.5
CONTRAST RATIO	See note 3			Minor	2.5
RESPONSE TIME	See note 1			Minor	2.5

7-6 Reliability

The LCD module should have no failure in the following reliability test.

TEST ITEM	*TEST CONDITIONS*	*NOTE*
HIGH TEMPERATURE STORAGE	60°C , 200 hr.	NOTE
LOW TEMPERATURE STORAGE	-10°C , 200 hr.	NOTE
HUMIDITY STORAGE	60°C , 90%RH , 96hr.	NOTE
HIGH TEMPERATURE OPERATION	40°C, typical operating conditions, 200hr.	NOTE
TEMPERATURE CYCLING	-10°C~70°C 10min. between each step temp. 50min. at each step temp. 5 cycles.	NOTE
MECHANICAL VIBRATION	10~55Hz sweep, 3G. amp1 =10mm(max) XYZ for 10min. each.	NOTE

NOTE 1: The module should not have condensation of water on the module.

NOTE 2: The module shelled be inspected after 1 hour storage in normal conditions (15~35^{O}C, 45~65%RH).

DEFINITIONS OF LIFE END POINT:

(1) Current drain should be smaller than the specified value.

(2) Function of the module should be maintained.

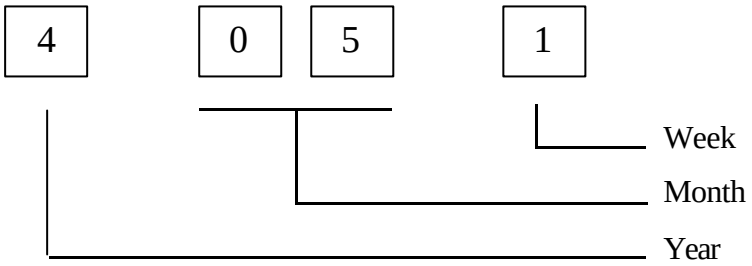
(3) Appearance and display quality should not have distinguished degradation.

(4) Contrast ratio should be larger than 50% of initial value.

8. Designation of lot mark

8-1 Lot mark

Lot mark is consisted of 4 digit number.



YEAR	FIGURE IN LOT MARK
1989	9
1990	0
1991	1
1992	2
1993	3
1994	4

MONTH	FIGURE IN LOT MARK	MONTH	FIGURE IN LOT MARK
Jan.	01	July	07
Feb.	02	Aug.	08
Mar.	03	Sept.	09
Apr.	04	Oct.	10
MAY	05	Nov.	11
Jun.	06	Dec.	12

WEEK (DAY IN CALENDAR)	FIGURE IN LOT MARK
1~7	1
8~14	2
15~21	3
22~28	4
29~31	5