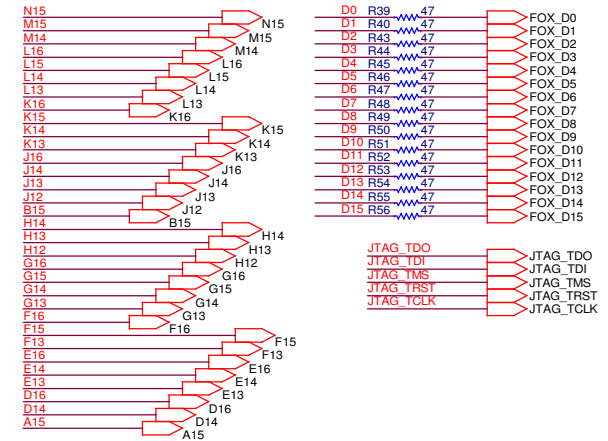


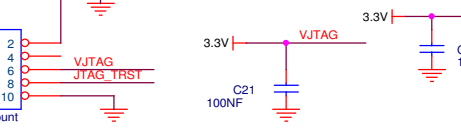
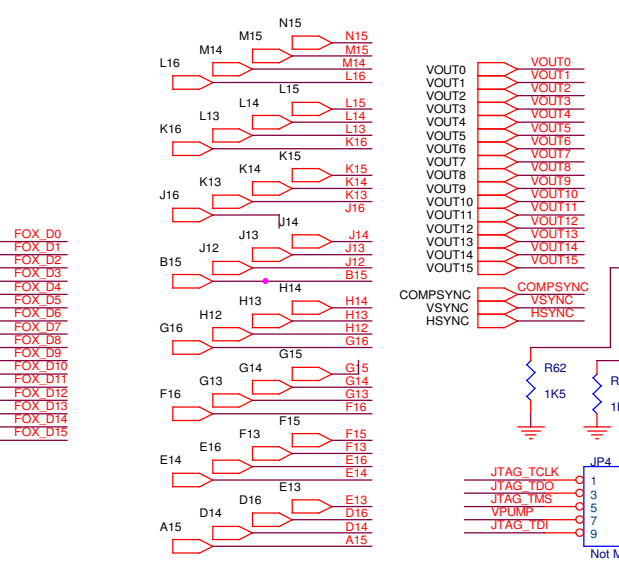
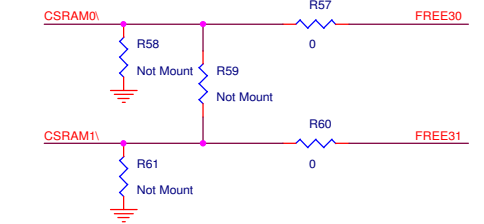
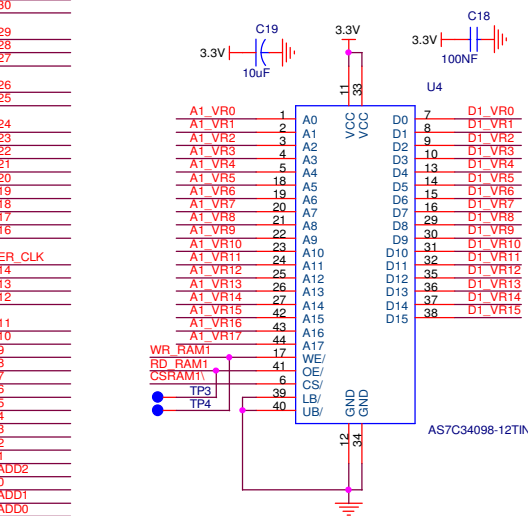
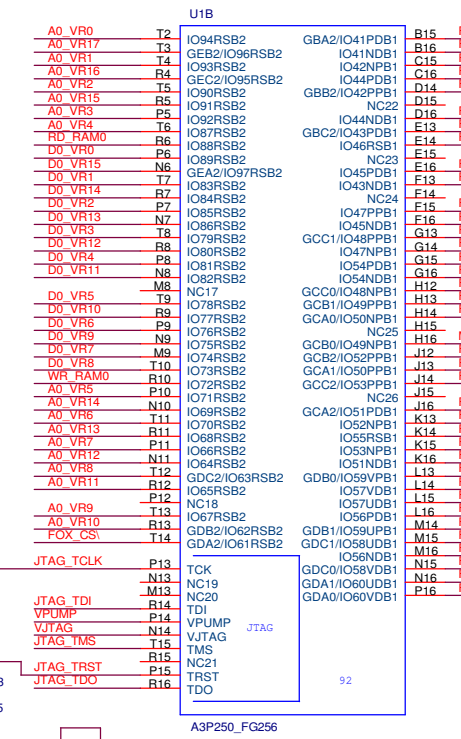
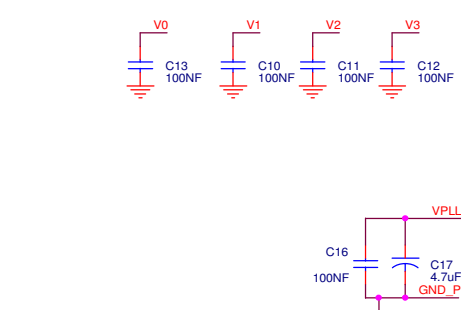
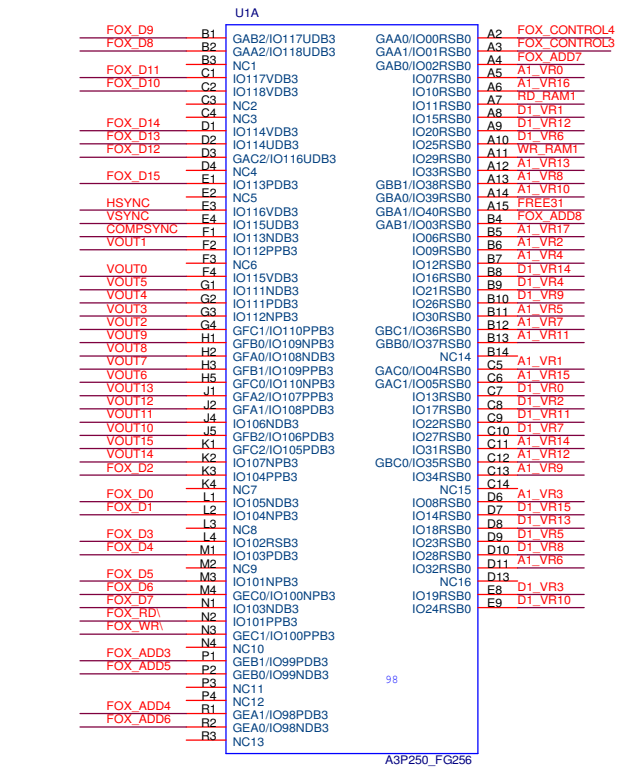
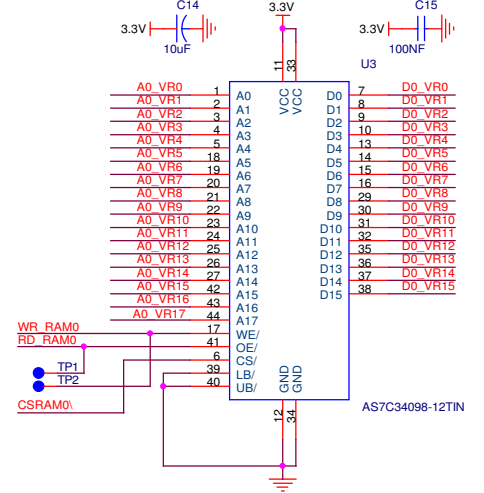
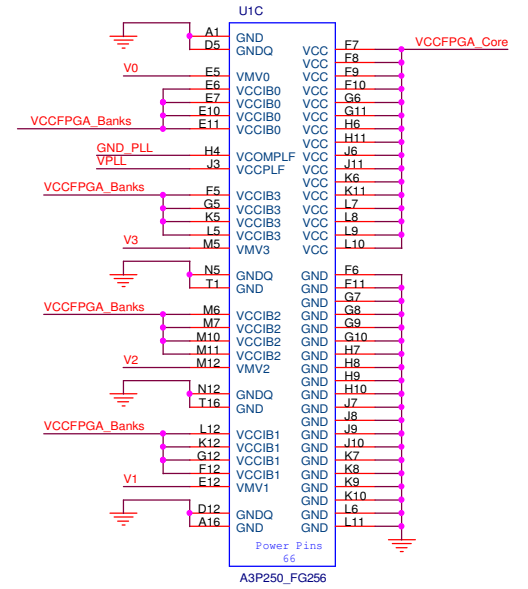
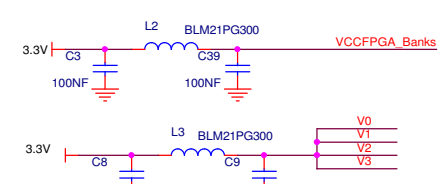
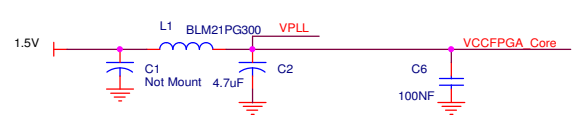
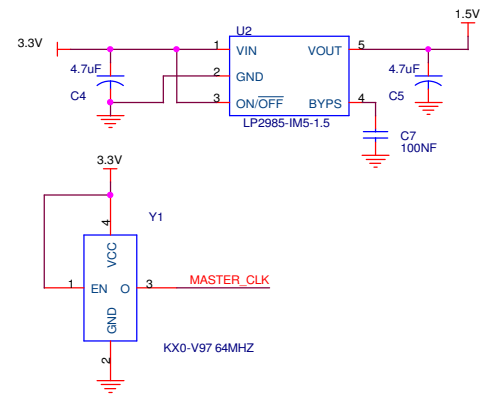
These names correspond to FPGA pins



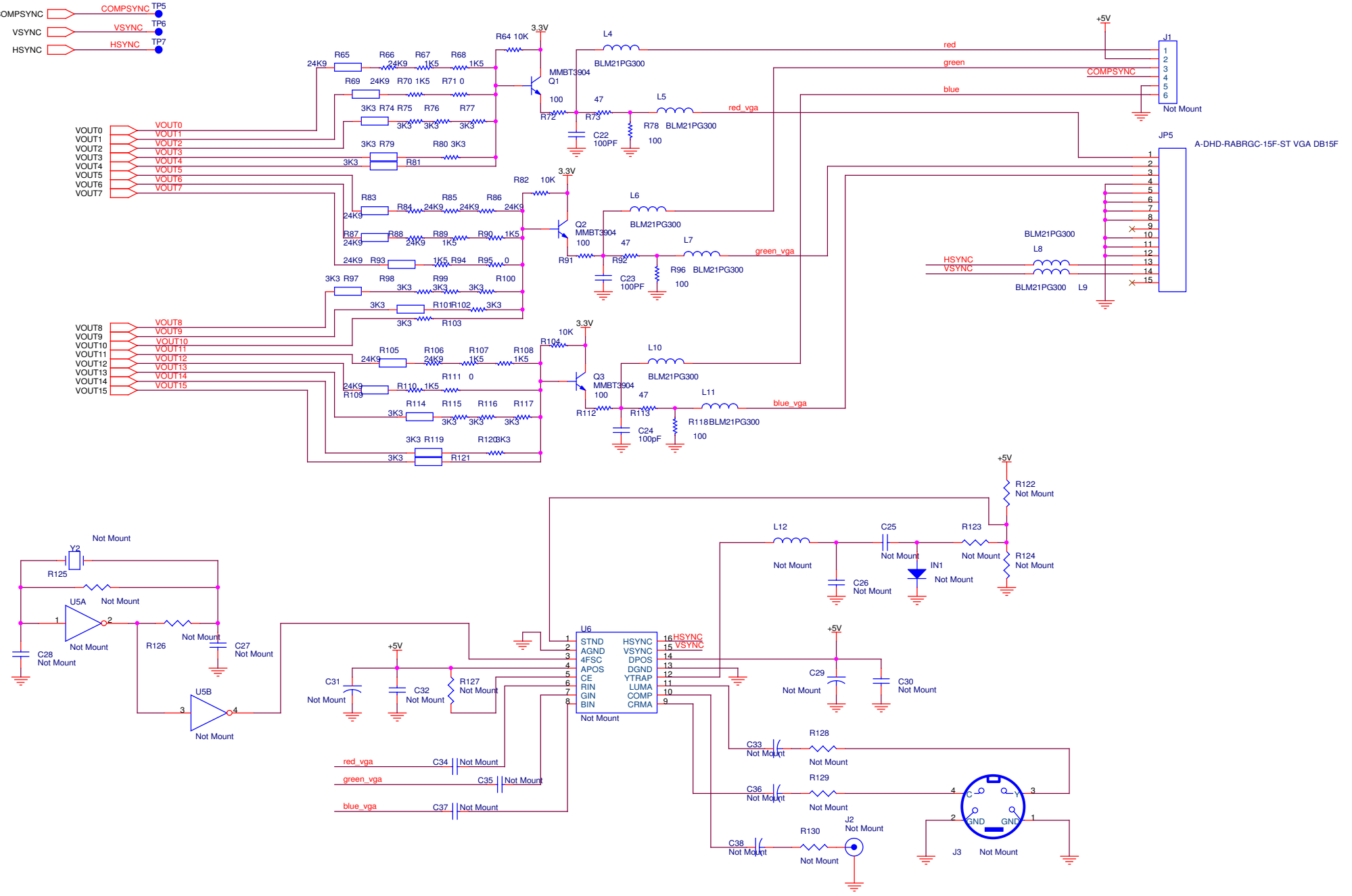
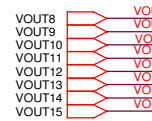
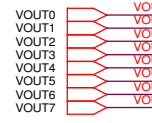
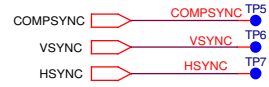
J6 and J7 correspond to Fox board top view

The power supplies sources are explicited: beware! +3.3V
max 500 mA

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